26.1 A 3-GHz 70Mb SRAM in 65nm CMOS Technology with Integrated Column-Based Dynamic Power Supply

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CMOS technology scaling makes it increasingly difficult to achieve adequate SRAM cell stability for low power applications. Using multiple-power supplies has been proposed as an effective means to improve cell stability and/or reduce standby leakage power [1-3]. A common drawback in the prior work is that power supplies are implemented statically or along the wordline direction where Read and Write may happen simultaneously. That makes it very difficult to improve both read and write margins in large SRAMs where column interleaving is often required for area efficiency and soft-error reduction. In this work, a column based dynamic power supply (VCC) scheme is proposed and integrated into an SRAM design in a high-performance 65nm CMOS technology [4]. This scheme allows the SRAM cell voltage to be switched dynamically based on the actual read, write, or standby operation leading to improved cell margins in both Read and Write while minimizing the leakage power.

One of the most critical challenges in designing SRAM cells on sub-100nm technologies is to achieve balanced read and write margins. Optimizing the read and write imposes conflicting requirements on the cell design and becomes very difficult to balance the two by conventional device sizing and Vt optimization. The dynamic VCC switching introduced in this design helps break the "deadlock" between the read and write. During the read, a higher VCC is connected to the memory cells. It creates a positive voltage differential between the cell and WL and effectively increases the cell static noise margin (SNM) or the read stability. During write, a lower voltage is switched to the memory cells that are to be written effectively creating a negative voltage differential between the memory cell and the WL, making the cell easier to flip.

A 70Mb SRAM chip is composed of subarrays with the configuration as shown in Fig. 26.1.1. Each subarray has four banks with 128 rows × 128 columns along with a built-in 8:1 column MUX optimized for both performance and array efficiency [5]. At the edge of each bank, a VCC MUX is inserted between two global power supplies and the local power rail along each column. The MUX can pick one of the two power supplies, labeled as VCC_hi and VCC_lo, to connect to the array along the column direction. During the read operation, all columns of the entire bank are switched to VCC_hi to achieve better read stability, regardless of which specific column within the eight column group is actually read. During the Write operation, seven out of eight interleaved columns that are not being written but under "dummy read" stress are switched to VCC_hi while the column that is actually written is connected to VCC_lo, as illustrated in Fig. 26.1.2. When the bank is not being accessed, VCC_lo is always selected to minimize the leakage power. This power control is implemented at the bank level to achieve optimal power reduction since the bank is the minimum addressable unit. Figure 26.1.3 provides a block diagram of the dynamic VCC control circuits along with critical timings. The signals of Read, Write, Bank, along with Column Address [2:0], are used to determine which power supply is selected for each column. A global enable for VCC switching is also incorporated in the control logic. It is important to point out that the multi-VCC select signals need to be established early so the local VCC is stabilized before the WL is turned on. The VCC MUX control signals also need to remain valid for two cycles to ensure the correct power supply is maintained throughout the active cycles. To meet the timing requirements and achieve a clock-edge based synchronization, simple cycle-extension circuits are used on the key control signals such as Read and Write to enable the two-cycle duration. A PMOS latch that is controlled by the WL enable signal is introduced immediately after the control logic to ensure the local interlocking between the back-edge of the WL and the "de-select" of the power supply MUX. A voltage level shifter is also required when the peripheral circuits are connected to the lower power supply to completely shut off one of the two PMOS pass-gates within the MUX. The entire design is implemented in a static CMOS circuit to minimize switching power.

A 70Mb SRAM that contains column redundancy, electrical-programmable fuse, Phase-Lock-Loop (PLL), Programmable Built-In-Self-Test (PBIST) is built and packaged in an 8-metal layer Land-Grid-Array (LGA) package with a flip-chip technology. The die photo is shown in Fig. 26.1.7. Two power supplies are brought in from external pins with distributed global routing in the package and on the die. A measured frequency schmoo is shown in Fig. 26.1.4. The design has achieved a 3Ghz operating frequency with a 1.1V power supply. Figure 26.1.5 shows two infrared pictures of the die when the SRAM is undergoing Read and Write. The bank in idle is shown as the "dark" region since the lower power supply suppresses the photon emission. Contrast is also seen between columns being written ("dark") and columns under "dummy read" (bright) due to the voltage difference. The dynamic VCC design for cell stability improvement is demonstrated by a significant reduction in random single bit failures measured on silicon, as shown in Fig. 26.1.6.

A column-based dynamic power supply scheme is integrated into a high-frequency subarray design for logic applications. The dynamic power supply switching is proven to be effective in achieving good cell margin in both Read and Write while lowering the overall SRAM leakage power.

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Reference:
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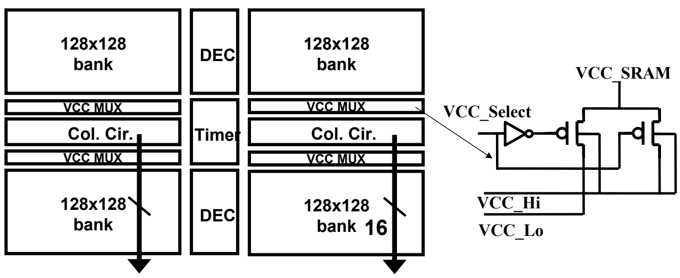

Figure 26.1.1: Subarray configuration with built-in VCC MUX.

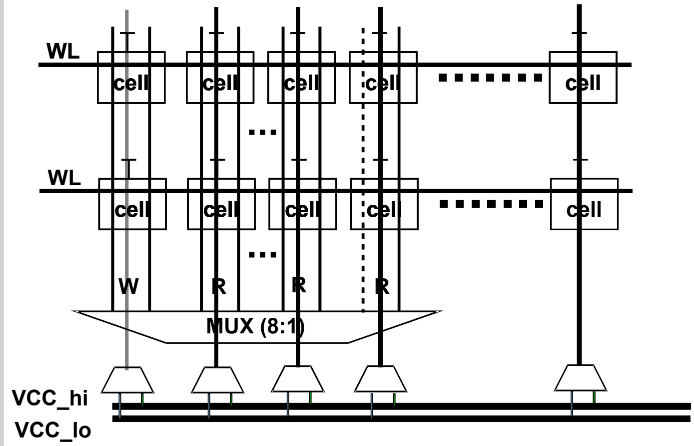

Figure 26.1.2: MUXing power supplies based on Read or Write.

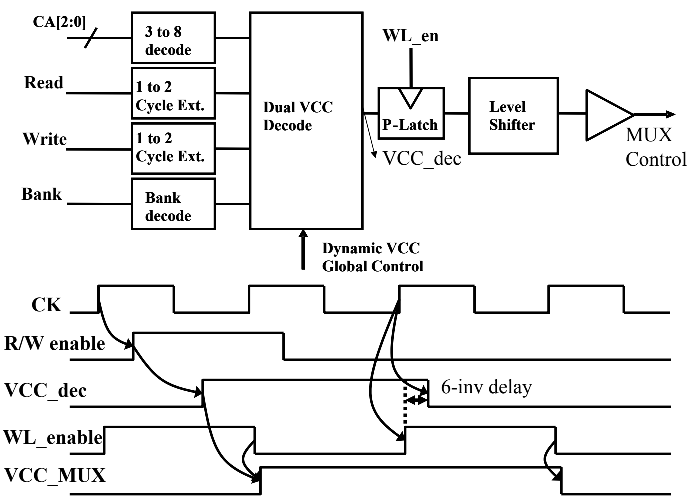

Figure 26.1.3: Dynamic VCC control logic and critical timing.

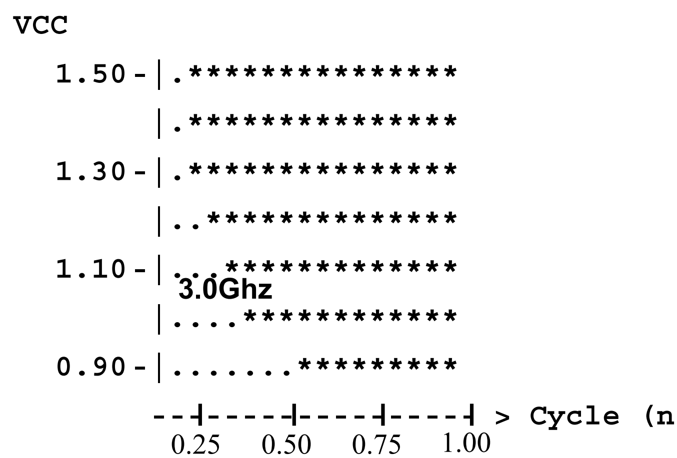

Figure 26.1.4: Measured voltage and frequency schmoo.

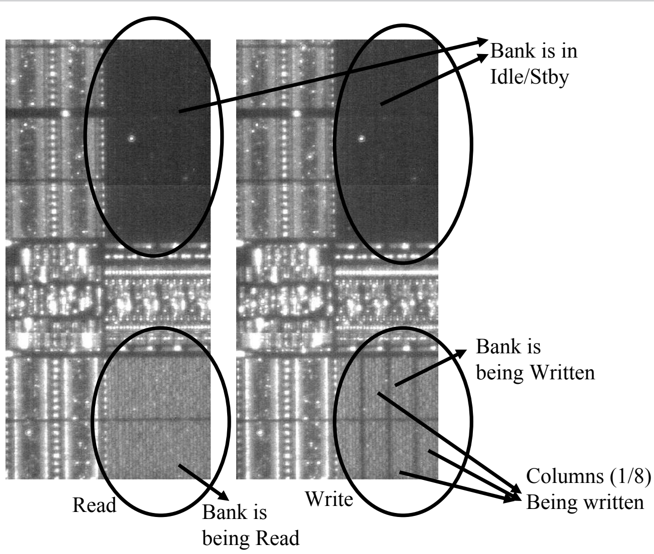

Figure 26.1.5: Infrared pictures of subarrays with dynamic VCC switching.

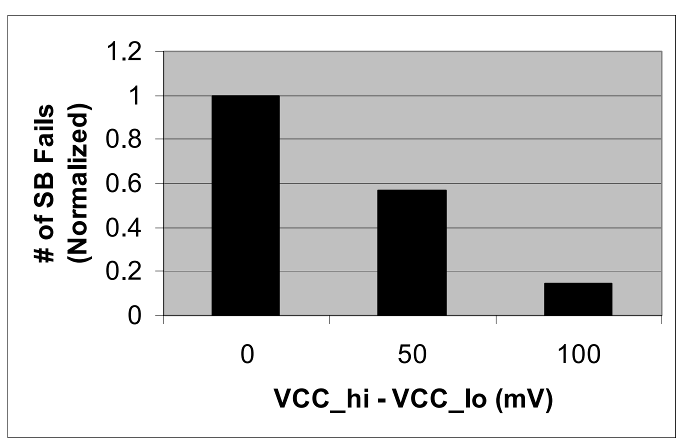

Figure 26.1.6: Measured reduction in random single bit failures with higher Read VCC.

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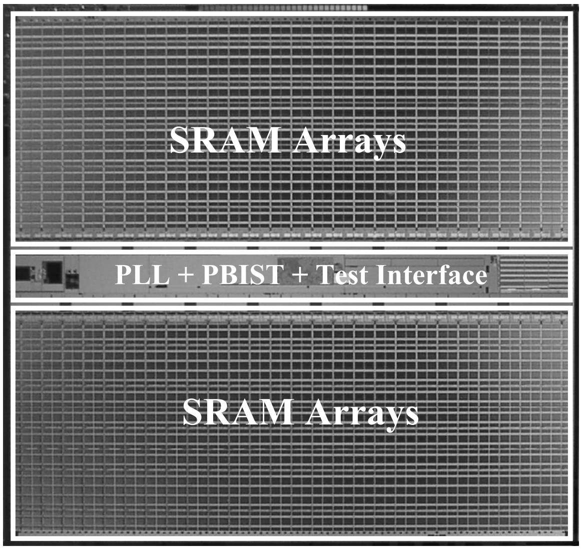

Figure 26.1.7: Chip Micrograph.

